REMARKS

Amended Claims

Claims 10, 12 and 13 are amended herein.

In the Drawings

The Examiner in the Non-final Office Action mailed April 20, 2006 stated that the drawings were disapproved for failing to comply with 37 C.F.R. §1.84(u)(1). The Examiner stated that the drawing views were required to be labeled "FIG." by 37 C.F.R. §1.84(u)(1) instead of the Applicant's "Fig." labeling.

Applicant notes that 37 C.F.R. §1.84(u)(1) only states that the drawing views be labeled with the term "Fig." And, while it uses an all capitalized form, does not explicitly state or require this. The Applicant further notes that MPEP §507(E) states that the drawing views should only be required to include the Applicant's form of label "Fig." and also does not require the all capitalized form insisted upon by the Examiner. The Applicant therefore respectfully maintains that given the lack of an explicit requirement for labeling and in view of the inconsistent requirements of 37 C.F.R. §1.84(u)(1) and MPEP §507(E), the Examiner's insistence on a given labeling style is not supported by 37 C.F.R. and the MPEP. Applicant thus respectfully requests that the Examiner's objection to the drawings be withdrawn and the drawings approved.

Claim Objections

Claims 10 and 13 were objected to due to informalities. The Examiner specifically objected to the phrasing of claims 10 and 13 "since the non-volatile memory is one of the types listed in the claim, not the whole non-volatile memory device as claimed."

Applicant has amended claims 10 and 13 herein to clarify what is claimed. Specifically claim 10 was amended to clarify that it is the type of non-volatile memory array utilized in the non-volatile memory device that is selected from the listed memory array types. Claim 13 was amended to clarify that the non-volatile memory device is adapted to act as a BIOS boot memory device. Accordingly, Applicant respectfully requests the withdrawal of the objection and reconsideration of claims 10 and 13.

Claim Rejections Under 35 U.S.C. § 112

Claim 12 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 12 has been amended to overcome the rejection under 35 U.S.C. §112, second paragraph. Specifically, claim 12 has been amended to clarify the antecedent basis of "the non-volatile memory" of line 1 as referring to the non-volatile memory device of claim 11, and this non-volatile memory device as being adapted to present one of the listed types of memory interfaces and present as a compatible memory device of that memory type through the synchronous interface. As such, the Applicant therefore respectfully requests that the rejection of claim 12 under 35 U.S.C. § 112, second paragraph be withdrawn as claim 12, as amended, has proper antecedent basis and clearly define the claimed invention.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 10-13, 17-22, 27-28, 34-35, 39-46, 52, 54-61, 67-68, 70-75, 79-80, 86-87 and 89-99 were rejected under 35 U.S.C. § 102(e) as being anticipated by Zitlaw et al. (U.S. Patent Publication No. 2004-0128425). Applicant respectfully traverses this rejection and requests reconsideration of the claims. Applicant reserves the right to swear behind the reference Roohparvar, but feels that claims 1, 10-13, 17-22, 27-28, 34-35, 39-46, 52, 54-61, 67-68, 70-75, 79-80, 86-87 and 89-99 are allowable for the following reasons.

Applicant respectfully maintains that in Figure 1B, Zitlaw et al. only discloses a system 150 having processor or controller 152 with a SDRAM memory bus 154, wherein the SDRAM memory bus 154 has a SyncFlash memory device 158 and several SDRAM DRAM memory devices 156, 160 coupled to it. As disclosed in Paragraphs [0008]-[0009] and [0036]-[0037], the system 150 is a computer or memory subsystem itself that has a SDRAM memory bus 154 used to access the coupled memory devices 156, 158, 160. Zitlaw et al. does not teach or disclose that the system 150 presents itself, and the coupled memory devices 156, 158, 160, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that Zitlaw et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory

arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Zitlaw et al., Abstract; Figures 1A and 1B; Paragraphs [0008]-[0009] and [0036]-[0037].

In addition, as disclosed in Paragraph [0006] of Zitlaw et al., the SyncFlash memory device 158 is a Flash memory device that itself has a SDRAM compatible interface and control circuitry to allow itself to be utilized in a SDRAM memory bus; the controller 152 does not have to provide and manage an SDRAM interface for it, it already has one. *See, e.g.*, Zitlaw et al., Figure 1B and Paragraph [0006].

Applicant notes that in this Office Action the Examiner seems to interchangeably use memory array and memory device, and respectfully maintains that one skilled in the art would recognize them as not being interchangeable and that memory devices internally contain memory arrays and the control circuitry to support them.

The Examiner also stated that "Zitlaw teaches that the controller is adapted to selectively couple the DRAM memory array (using the chip select lines) to the synchronous memory interface; and selectively copy data from the non-volatile memory array and remap addresses of one or more DRAM memory array section to the synchronous memory interface to operate as 'shadow' memory (e.g. see paragraph [0008])" and that "Zitlaw teaches that the controller is adapted to operate the DRAM memory array (i.e. 160 in Fig. 1B) as (i) an extended read and/or write data buffer memory (i.e. 156 in Fig. 1B); and (ii) as 'scratch pad' memory, i.e. the temporary or cache memory (e.g. see paragraph [0008] and Fig. 1B)." (Office Action mailed on April 20, 2006, Pages 6-7).

Applicant has carefully reviewed Zitlaw et al. and, in particular, Paragraph [0008] of Zitlaw et al., and can find no mention of the controller remapping addresses of one or more DRAM memory array sections to the synchronous memory interface to operate as "shadow" memory, or the utilization of the DRAM as an extended read and/or write data buffer memory, "scratch pad" memory, or temporary or cache memory. Applicant therefore respectfully maintains that Zitlaw et al. does not disclose using the DRAM memory devices as a buffer memory "shadow" memory, scratch pad" memory, temporary or cache memory, or the controller being adapted to use the SDRAM as such.

Applicant therefore respectfully submits that Zitlaw et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. Applicant thus respectfully submits that Zitlaw et al. does not teach or disclose all elements of the Applicant's claimed invention.

Furthermore, Applicant respectfully calls attention to 35 U.S.C. § 103(c) which indicates that Zitlaw et al., being available as a reference only under 35 U.S.C. § 102(e), may not be used as a basis for a § 103 rejection being commonly assigned to the same entity as the current application at the time of invention.

Applicant's claim 1, recites, "[a] non-volatile memory device comprising: a non-volatile memory array; a buffer memory; a synchronous memory interface; and a controller coupled to the non-volatile memory array, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and buffer memory and to present the non-volatile memory device as a synchronous memory device through the synchronous memory interface." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a non-volatile memory device having a controller, a non-volatile memory array, a buffer memory, and a synchronous memory interface, wherein the controller is adapted to manage and present the non-volatile memory array and buffer memory through the synchronous interface as a synchronous memory device. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 1.

Applicant's claim 22, recites, "[a] NAND architecture Flash memory device comprising: a NAND architecture Flash memory array; a buffer memory; a synchronous memory interface; and a controller coupled to the NAND architecture Flash memory array, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the NAND architecture Flash memory array and to portray the NAND architecture Flash memory device as a synchronous memory device through the synchronous memory interface." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a NAND architecture Flash memory device having a controller, a NAND architecture Flash memory array, a buffer memory, and a synchronous memory interface, wherein the controller is adapted to

manage and present the NAND architecture Flash memory array and buffer memory through the synchronous interface as a synchronous memory device. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 22.

Applicant's claim 27, recites, "[a] non-volatile memory subsystem comprising: one or more non-volatile memory devices; a buffer memory; a synchronous memory interface; and a controller coupled to the one or more non-volatile memory devices, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory devices and to present the non-volatile memory devices as a synchronous memory device through the synchronous memory interface." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a non-volatile memory subsystem having a controller, one or more non-volatile memory devices, a buffer memory, and a synchronous memory interface, wherein the controller is adapted to manage and present the one or more non-volatile memory devices and buffer memory through the synchronous interface as a synchronous memory device. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 27.

Applicant's claim 45, recites, "[a] system comprising: a host; and one or more non-volatile memory devices coupled to the host, wherein each of the one or more non-volatile memory devices comprises, a non-volatile memory array; a buffer memory; a synchronous memory interface; and a controller coupled to the non-volatile memory array, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and to present the non-volatile memory device as a synchronous memory device through the synchronous memory interface." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a system. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 45.

Applicant's claim 60, recites, "[a] method of operating a non-volatile memory device comprising: managing the non-volatile memory device with an internal controller; presenting the non-volatile memory device as a synchronous memory device through a synchronous memory interface; and buffering data access requests received through the synchronous memory interface in an internal buffer memory." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a method of operating a non-volatile memory device. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 60.

Applicant's claim 75, recites, "[a] method of operating a NAND architecture Flash memory device comprising: managing the NAND architecture Flash memory device with an internal controller; presenting the NAND architecture Flash memory device as a synchronous memory device through a synchronous memory interface; and buffering data access requests received through the synchronous memory interface in an internal buffer memory." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a method of operating a NAND architecture Flash memory device. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 75.

Applicant's claim 94, recites, "[a] machine-usable medium, the machine-usable medium containing a software routine for causing a memory controller to execute a method, wherein the method comprises: managing one or more non-volatile memory devices with the memory controller; presenting one or more non-volatile memory devices as a synchronous memory device through a synchronous memory interface; and buffering data access requests received through the synchronous memory interface in a buffer memory." As detailed above, Applicant submits that Zitlaw et al. fails to teach or disclose such a machine-usable medium and method. As such, Zitlaw et al. fails to teach or disclose all elements of independent claim 94.

Applicant respectfully contends that claims 1, 22, 27, 45, 60, 75, and 94 as pending have been shown to be patentably distinct from the cited reference of Zitlaw et al. As claims 10-13, 17-21, 28, 34-35, 39-44, 46, 52, 54-59, 61, 67-68, 70-74, 79-80, 86-87, 89-93, and 95-99 depend from and further define claims 1, 17, 29, 40, and 48, respectively, they are also believed to be allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 1, 10-13, 17-22, 27-28, 34-35, 39-46, 52, 54-61, 67-68, 70-75, 79-80, 86-87 and 89-99.

Claim Rejections Under 35 U.S.C. § 103

Claims 2-4, 6-7, 23-26, 29-31, 47-49, 62, 65, 76, 78, 81 and 84 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zitlaw et al. in view of McCormack et al. (U.S. Patent No. 5,781,201). Applicant respectfully traverses this rejection and feels that claims 2-4, 6-7, 23-26, 29-31, 47-49, 62, 65, 76, 78, 81 and 84 are allowable for the following reasons.

Applicant respectfully maintains, as stated above in regards to the rejection of independent claims 1, 22, 27, 45, 60, and 75, from which claims 2-4, 6-7, 23-26, 29-31, 47-49,

62, 65, 76, 78, 81 and 84 depend, Zitlaw et al. only discloses a system 150 having processor or controller 152 with a SDRAM memory bus 154, wherein the SDRAM memory bus 154 has a SyncFlash memory device 158 and several SDRAM DRAM memory devices 156, 160 coupled to it. As disclosed in Paragraphs [0008]-[0009] and [0036]-[0037], the system 150 is a computer or memory subsystem itself that has a SDRAM memory bus 154 used to access the coupled memory devices 156, 158, 160. Zitlaw et al. does not teach or disclose that the system 150 presents itself, and the coupled memory devices 156, 158, 160, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that Zitlaw et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Zitlaw et al., Abstract; Figures 1A and 1B; Paragraphs [0008]-[0009] and [0036]-[0037].

Furthermore, Applicant respectfully calls attention to 35 U.S.C. § 103(c) which indicates that Zitlaw et al., being available as a reference only under 35 U.S.C. § 102(e), may not be used as a basis for a § 103 rejection being commonly assigned to the same entity as the current application at the time of invention.

In addition, Applicant respectfully maintains that McCormack et al. discloses a method of read and write buffering to a video memory to allow for maximum bus utilization. Applicant therefore respectfully submits that McCormack et al. does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, McCormack et al., Abstract.

Applicant thus respectfully submits that combining Zitlaw et al. with McCormack et al. does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that Zitlaw et al. and McCormack et al. do not teach or

suggest all elements of Applicant's claims 1, 22, 27, 45, 60, and 75, either alone or in combination.

As such, Applicant respectfully contends that claims 1, 22, 27, 45, 60, and 75 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 2-4, 6-7, 23-26, 29-31, 47-49, 62, 65, 76, 78, 81 and 84 depend from and further define claims 1, 22, 27, 45, 60, and 75, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 2-4, 6-7, 23-26, 29-31, 47-49, 62, 65, 76, 78, 81 and 84.

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Zitlaw et al. in view of McCormack, further in view of Widdup (U.S. Patent No. 6,651,148). Applicant respectfully traverses this rejection and feels that claim 5is allowable for the following reasons.

Applicant respectfully maintains, as stated above in regards to the rejection of independent claim 1, from which claim 5 depends, Zitlaw et al. only discloses a system 150 having processor or controller 152 with a SDRAM memory bus 154, wherein the SDRAM memory bus 154 has a SyncFlash memory device 158 and several SDRAM DRAM memory devices 156, 160 coupled to it. As disclosed in Paragraphs [0008]-[0009] and [0036]-[0037], the system 150 is a computer or memory subsystem itself that has a SDRAM memory bus 154 used to access the coupled memory devices 156, 158, 160. Zitlaw et al. does not teach or disclose that the system 150 presents itself, and the coupled memory devices 156, 158, 160, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that Zitlaw et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Zitlaw et al., Abstract; Figures 1A and 1B; Paragraphs [0008]-[0009] and [0036]-[0037].

Furthermore, Applicant respectfully calls attention to 35 U.S.C. § 103(c) which indicates that Zitlaw et al., being available as a reference only under 35 U.S.C. § 102(e), may not be used

as a basis for a § 103 rejection being commonly assigned to the same entity as the current application at the time of invention.

In addition, Applicant respectfully maintains that McCormack et al. discloses a method of read and write buffering to a video memory to allow for maximum bus utilization. *See, e.g.*, McCormack et al., Abstract.

Further, Applicant respectfully maintains that Widdup discloses a memory controller that incorporates a read and write arbiter to allow pseudo-simultaneous memory transactions. Applicant therefore respectfully submits that Widdup does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Widdup, Abstract; column 4, line 65 to column 5, line 11.

Applicant thus respectfully submits that combining Zitlaw et al. and McCormack et al. with Widdup does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that Zitlaw et al., McCormack et al. and Widdup do not teach or suggest all elements of Applicant's claim 1, either alone or in combination.

As such, Applicant respectfully contends that claim 1 as pending has been shown to be patentably distinct from the cited references, either alone or in combination. As claim 5 depends from and further define claim 1, it is also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claim 5.

Claims 8, 32, 50, 63-64, 77 and 82-83 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zitlaw et al. in view of McCormack, further in view of Wallace et al. (U.S. Patent No. 6,628, 537). Applicant respectfully traverses this rejection and feels that claims 8, 32, 50, 63-64, 77 and 82-83 are allowable for the following reasons.

Applicant respectfully maintains, as stated above in regards to the rejection of independent claims 1, 27, 45, 60, and 75, from which claims 8, 32, 50, 63-64, 77 and 82-83

depend, Zitlaw et al. only discloses a system 150 having processor or controller 152 with a SDRAM memory bus 154, wherein the SDRAM memory bus 154 has a SyncFlash memory device 158 and several SDRAM DRAM memory devices 156, 160 coupled to it. As disclosed in Paragraphs [0008]-[0009] and [0036]-[0037], the system 150 is a computer or memory subsystem itself that has a SDRAM memory bus 154 used to access the coupled memory devices 156, 158, 160. Zitlaw et al. does not teach or disclose that the system 150 presents itself, and the coupled memory devices 156, 158, 160, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that Zitlaw et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Zitlaw et al., Abstract; Figures 1A and 1B; Paragraphs [0008]-[0009] and [0036]-[0037].

Furthermore, Applicant respectfully calls attention to 35 U.S.C. § 103(c) which indicates that Zitlaw et al., being available as a reference only under 35 U.S.C. § 102(e), may not be used as a basis for a § 103 rejection being commonly assigned to the same entity as the current application at the time of invention.

In addition, Applicant respectfully maintains that McCormack et al. discloses a method of read and write buffering to a video memory to allow for maximum bus utilization. *See, e.g.*, McCormack et al., Abstract. Further, Applicant respectfully maintains that Wallace et al. discloses a computer memory card that writes a BUSY signal into a status register and does not teach or disclose a READY/BUSY pin. Applicant therefore respectfully submits that Wallace et al. does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Wallace et al., Abstract; Figure 16, column 9, line 65 to column 10, line 40.

Applicant thus respectfully submits that combining Zitlaw et al. and McCormack et al. with Wallace et al. does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that Zitlaw et al., McCormack et al. and Wallace et al. do not teach or suggest all elements of Applicant's claims 1, 27, 45, 60, and 75, either alone or in combination.

As such, Applicant respectfully contends that claims 1, 27, 45, 60, and 75 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 8, 32, 50, 63-64, 77 and 82-83 depend from and further define claims 1, 27, 45, 60, and 75, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 8, 32, 50, 63-64, 77 and 82-83.

Claims 9, 33, 51, 66 and 85 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zitlaw et al. in view Meyer (U.S. Patent No. 4,065,862). Applicant respectfully traverses this rejection and feels that claims 9, 33, 51, 66 and 85 are allowable for the following reasons.

Applicant respectfully maintains, as stated above in regards to the rejection of independent claims 1, 27, 45, 60, and 75, from which claims 9, 33, 51, 66 and 85 depend, Zitlaw et al. only discloses a system 150 having processor or controller 152 with a SDRAM memory bus 154, wherein the SDRAM memory bus 154 has a SyncFlash memory device 158 and several SDRAM DRAM memory devices 156, 160 coupled to it. As disclosed in Paragraphs [0008]-[0009] and [0036]-[0037], the system 150 is a computer or memory subsystem itself that has a SDRAM memory bus 154 used to access the coupled memory devices 156, 158, 160. Zitlaw et al. does not teach or disclose that the system 150 presents itself, and the coupled memory devices 156, 158, 160, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that Zitlaw et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device.

See, e.g., Zitlaw et al., Abstract; Figures 1A and 1B; Paragraphs [0008]-[0009] and [0036]-[0037].

Furthermore, Applicant respectfully calls attention to 35 U.S.C. § 103(c) which indicates that Zitlaw et al., being available as a reference only under 35 U.S.C. § 102(e), may not be used as a basis for a § 103 rejection being commonly assigned to the same entity as the current application at the time of invention.

In addition, Applicant respectfully maintains that Meyer discloses an interface and method for synchronizing data signals and clock pulses across a data transmission system, such as a RS-232-C serial line, disclosing a "BUFFER FULL" signal line. Applicant maintains that Meyer does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Meyer, Figures 1 and 2, Abstract; column 1, line 12 to column 4, line 25.

Applicant thus respectfully submits that combining Zitlaw et al. with Meyer does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that Zitlaw et al. and Meyer do not teach or suggest all elements of Applicant's claims 1, 27, 45, 60, and 75, either alone or in combination.

As such, Applicant respectfully contends that claims 1, 27, 45, 60, and 75 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 9, 33, 51, 66 and 85 depend from and further define claims 1, 27, 45, 60, and 75, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 9, 33, 51, 66 and 85.

Claims 14 and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zitlaw et al. in view of Bartoli et al. (U.S. Patent No. 6,442,068). Applicant respectfully traverses this rejection and feels that claims 14 and 36 are allowable for the following reasons.

Applicant respectfully maintains, as stated above in regards to the rejection of independent claims 1 and 27, from which claims 14 and 36 depend, Zitlaw et al. only discloses a

system 150 having processor or controller 152 with a SDRAM memory bus 154, wherein the SDRAM memory bus 154 has a SyncFlash memory device 158 and several SDRAM DRAM memory devices 156, 160 coupled to it. As disclosed in Paragraphs [0008]-[0009] and [0036]-[0037], the system 150 is a computer or memory subsystem itself that has a SDRAM memory bus 154 used to access the coupled memory devices 156, 158, 160. Zitlaw et al. does not teach or disclose that the system 150 presents itself, and the coupled memory devices 156, 158, 160, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that Zitlaw et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Zitlaw et al., Abstract; Figures 1A and 1B; Paragraphs [0008]-[0009] and [0036]-[0037].

Furthermore, Applicant respectfully calls attention to 35 U.S.C. § 103(c) which indicates that Zitlaw et al., being available as a reference only under 35 U.S.C. § 102(e), may not be used as a basis for a § 103 rejection being commonly assigned to the same entity as the current application at the time of invention.

In addition, Applicant respectfully maintains that Bartoli et al. discloses a non-volatile memory having the capability to suspend a programming or erase operation to conduct a burst or page mode read, and does not disclose or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Bartoli et al., Abstract; Summary.

Applicant thus respectfully submits that combining Zitlaw et al. with Bartoli et al. does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that Zitlaw et al. and Bartoli et al. do not teach or suggest all elements of Applicant's claims 1 and 27, either alone or in combination.

As such, Applicant respectfully contends that claims 1 and 27 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 14 and 36 depend from and further define claims 1 and 27, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 14 and 36.

Claims 15-16, 37-38, 69 and 88 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zitlaw et al. in view of the 'Background of Invention' (BOI) section of the present application. Applicant respectfully traverses this rejection and feels that claims 15-16, 37-38, 69 and 88 are allowable for the following reasons.

Applicant respectfully maintains, as stated above in regards to the rejection of independent claims 1, 27, 60, and 75, from which claims 15-16, 37-38, 69 and 88 depend, Zitlaw et al. only discloses a system 150 having processor or controller 152 with a SDRAM memory bus 154, wherein the SDRAM memory bus 154 has a SyncFlash memory device 158 and several SDRAM DRAM memory devices 156, 160 coupled to it. As disclosed in Paragraphs [0008]-[0009] and [0036]-[0037], the system 150 is a computer or memory subsystem itself that has a SDRAM memory bus 154 used to access the coupled memory devices 156, 158, 160. Zitlaw et al. does not teach or disclose that the system 150 presents itself, and the coupled memory devices 156, 158, 160, through an external SDRAM interface as being a SDRAM device in its own right or as emulating a SDRAM DRAM. Applicant therefore respectfully submits that Zitlaw et al. does not teach or disclose a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. *See, e.g.*, Zitlaw et al., Abstract; Figures 1A and 1B; Paragraphs [0008]-[0009] and [0036]-[0037].

In addition, Applicant respectfully maintains that Paragraph [0005] of the BOI discloses only that to compensate for their higher error rates "and to take advantage of the inherent higher array density, NAND Flash memory typically utilizes error correction codes (ECC) and/or are

interfaced to and presented as a mass storage device, such as a magnetic disk. In this manner the errors of a NAND Flash memory device can be addressed by the operating system/host/driver/firmware and/or the file system that the Flash device is formatted with." *See*, BOI of Present Application, Paragraph [0005]. As such, Applicant maintains that the BOI does not teach or suggest a synchronous memory device or memory subsystem that has a controller, a synchronous interface, a buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays, wherein the controller is adapted to manage the buffer memory and one or more internal non-volatile memory devices or non-volatile memory arrays and present them through the synchronous interface as a synchronous memory device. Furthermore, Applicant respectfully maintains that the BOI, while disclosing the use of ECC codes in NAND Flash memory devices, does not teach or suggest ECC hardware incorporated with the NAND Flash memory device or that SDRAM DRAM's utilize ECC codes. Applicant respectfully maintains that ECC codes are not utilized in volatile DRAM memory devices, ECC codes are known by those skilled in the art to be too slow and inappropriate for the access speed and size of the data generally stored in DRAM, and that one skilled in the art would therefore not utilize ECC codes with a memory device that presented itself as a read/write compatible SDRAM.

Applicant thus respectfully submits that combining Zitlaw et al. with the BOI does not teach or suggest the Applicant's claimed invention, as maintained by the Examiner. Applicant therefore respectfully contends that Zitlaw et al. and the BOI do not teach or suggest all elements of Applicant's claims 1, 27, 60, and 75, either alone or in combination.

As such, Applicant respectfully contends that claims 1, 27, 60, and 75 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 15-16, 37-38, 69 and 88 depend from and further define claims 1, 27, 60, and 75, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 15-16, 37-38, 69 and 88.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 7/20/06

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